LESSON PLAN

Discipline: Electrical Engg.	**Semester:** Fifth(5th)	**Name of the Faculty:** Er. Biswaranjan Nayak
Subject: Digital Electronics & Microprocessor	**No of Days/week class** allotted: Five(5)	**Semester from Date:** 15.09.22 to 22.12.22
WEEK	**CLASS DAY**	**THEORY TOPICS**
1st	1st	**I**ntroduction.
	2nd	Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	3rd	Binary addition, subtraction, Multiplication and Division.
	4th	1‘s complement and 2‘s complement numbers for a binary number
	5th	Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421
2nd	1st	Excess-3 and Gray Code and vice-versa.
	2nd	Importance of parity Bit.
	3rd	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	4th	Realize AND, OR, NOT operations using NAND gates.
	5th	Realize AND, OR, NOT operations using NOR gates.
3rd	1st	Different postulates and De-Morgan‘s theorems in Boolean algebra.
	2nd	Use Of Boolean Algebra For Simplification Of Logic Expression
	3rd	Karnaugh Map For 2&3Variable,
	4th	Karnaugh Map For 4 Variable,
	5th	Simplification Of SOP And POS Logic Expression Using K-Map.
4th	1st	**Review Class**
	2nd	Give the concept of Combinational Logic circuit.
	3rd	Half adder circuit and verify its functionality using truth table.
	4th	Realize a Half-adder using NAND gates only and NOR gates only.
	5th	**Monthly Test**
5th	1st	Full adder circuit and explain its operation with truth table.
	2nd	Realize full-adder using two Half-adders and an OR – gate and write truth table
	3rd	Full subtractor circuit and explain its operation with truth table.
	4th	Operation of 4 X 1 Multiplexers and 1 X 4 DE multiplexer
	5th	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
6th	1st	Working of Two bit magnitude comparator.
	2nd	**Review Class**
	3rd	Give the Idea of the Sequential Logic Circuits
	4th	State the necessity of clock and give the concept of level clocking and edge triggering,
	5th	Clocked SR flip flop with preset and clear inputs.
7th	1st	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table.
	2nd	Concept of race around condition and study of master slave JK flip flop.

	3rd	Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	4th	Applications of flip flops.
	5th	**Monthly Test**
8th	1st	Define modulus of a counter
	2nd	4-bit asynchronous counter and its timing diagram.
	3rd	Asynchronous decade counter.
	4th	4-bit synchronous counter.
	5th	Distinguish between synchronous and asynchronous counters.
9th	1st	State the need for a Register and list the four types of registers.
	2nd	Working of SISO, SIPO, Register with truth table using flip flop.
	3rd	PISO, PIPO Register with truth table using flip flop
	4th	**Review Class**
	5th	Introduction to microprocessor and microcomputer
10th	1st	Architecture of Intel 8085A Microprocessor and description of each block.
	2nd	Pin diagram and description.
	3rd	Stack, Stack pointer & stack top
	4th	Interrupts
	5th	**Monthly Test**
11th	1st	Opcode & Operand
	2nd	Differentiate between one byte, two byte & three byte instruction with example.
	3rd	Instruction set of 8085 example
	4th	Addressing mode
	5th	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
12th	1st	Timing Diagram for memory read, memory write, I/O read, I/O write
	2nd	Timing Diagram for 8085 instruction
	3rd	Counter and time delay.
	4th	Simple assembly language programming of 8085.
	5th	Cont. .....
13th	1st	**Review Class**
	2nd	Basics Interfacing Concepts.
	3rd	Memory mapping & I/O mapping
	4th	Functional block diagram of Intel 8255
	5th	Description of each block of Programmable peripheral interface Intel 8255
14th	1st	Cont.
	2nd	Application using 8255: Seven segment LED display,
	3rd	**Monthly Test**
	4th	Square wave generator
	5th	Traffic light Controller
15th	1st	**Review Class**
	2nd	Revision class
	3rd	Revision class
	4th	Revision class
	5th	Revision class